IN THE CLAIMS:

The text of all pending claims (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

1. (CANCELED).

2. (PREVIOUSLY PRESENTED) The computer as claimed in claim 21, wherein said data holding part includes a plurality of registers.

3. (PREVIOUSLY PRESENTED) The computer as claimed in claim 2, said computer further comprising flags each of said flags indicating whether said data is held in said plurality of registers.

4. (PREVIOUSLY PRESENTED) The computer as claimed in claim 21, said computer further comprising a data storing part, wherein said data holding part holds said data to be stored in said data storing part at a time when said interrupt occurs while a store instruction is executed, said store instruction requesting that said data is stored in said data storing part.

5. (PREVIOUSLY PRESENTED) The computer as claimed in claim 21, wherein said data holding part holds an instruction address of an instruction which causes said interrupt.

6. (CANCELED).

7. (PREVIOUSLY PRESENTED) The computer as claimed in claim 21, wherein said data holding part holds an effective address of a load instruction or a store instruction when said interrupt occurs while said load instruction or said store instruction is executed.

8. (PREVIOUSLY PRESENTED) The computer as claimed in claim 21, wherein said data is used for recovery from said interrupt.

9. (CANCELED).

10. (PREVIOUSLY PRESENTED) The control method as claimed in claim 22, wherein said data is held in a plurality of registers and said data is used for recovery from a plurality of interrupts.

11. (PREVIOUSLY PRESENTED) The control method as claimed in claim 10, wherein flags are used in which each of which flags indicates whether said data is held in said plurality of registers.

12. (PREVIOUSLY PRESENTED) The control method as claimed in claim 22, said control method comprising:

holding said data to be stored in a data storing part in said computer at a time when said interrupt occurs while a store instruction is executed, said store instruction requesting that said data is stored in said data storing part.

13. (PREVIOUSLY PRESENTED) The control method as claimed in claim 22, said control method comprising:

holding an instruction address of an instruction which causes said interrupt.

14. (CANCELED).

15. (PREVIOUSLY PRESENTED) The control method as claimed in claim 22, said control method comprising:

holding an effective address of a load instruction or a store instruction when said interrupt occurs while said load instruction or said store instruction is executed.

16. (PREVIOUSLY PRESENTED) The control method as claimed in claim 22, wherein said data is used for recovery from said interrupt.

17. (CURRENTLY AMENDED) A computer processing method of plural instructions in parallel, and performing interrupt processing, comprising:

holding in a memory addresses of the plural instructions when the interrupt processing starts,

wherein the computer processing method performs interrupt processing by an interrupt

processing program by reading the addresses of the plural instructions from the memory to return from the interrupt.

18. (PREVIOUSLY PRESENTED) The computer processing method according to claim 17, further comprising continuing execution of the instructions based on the addresses held in the memory.

19. (CANCELLED)

20. (PREVIOUSLY PRESENTED) The computer processing method according to claim 18, wherein the interrupt processing is initiated by an exception operation.

21. (CURRENTLY AMENDED) A computer which processes plural instructions in parallel, and which performs an interrupt process when an interrupt occurs while an instruction in a program is executed, said computer comprising:

a data holding part holding data on all of instructions being executed at a time when said interrupt starts to occur,

wherein the computer performs interrupt processing by an interrupt processing program by reading the data from holding part to return from the interrupt.

22. (CURRENTLY AMENDED) A control method of a computer which processes plural instructions in parallel, and which performs an interrupt process when an interrupt occurs while an instruction in a program is executed, said method comprising:

holding data on all of instructions being executed at a time when said interrupt starts to occur,

wherein the control method performs interrupt processing by an interrupt processing program by reading the data from the held data to return from the interrupt.

23. (NEW) A method, comprising:

storing in a data holding unit all instructions being executed in parallel processing and interrupt processing instructions at a time when an interrupt starts; and

performing interrupt processing using the interrupt processing instructions stored in the data holding unit to return from the interrupt.